Development of Shunt Active Power Filter for Harmonic Reduction using Synchronous Reference Frame with Space Vector Pulse Width Modulation

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ABSTRACT: The work aims at development of Shunt Active Power Filter (SAPF) for harmonic reduction. The current harmonics are being caused by nonlinear characteristic of power electronics based equipments which increase power losses and in turn reduce power quality. Synchronous Reference Frame (SRF) was used as a control strategy and for reference harmonic current generation and Space Vector Pulse Width Modulation (SVPWM) was adopted as switching signal generation. With RL load under balanced input voltage condition, the developed SAPF-SVPWM achieved a reduction of THD of 0.91% as compared to 25.60 before compensation. In addition, the developed SAPF- SVPWM model was compared with SAPF without compensation using RL load under unbalanced voltage and the result shows that the developed SVPWM achieved reduction in THD of 1.74 % as compared to 26.68% after and before compensation. The developed SVPWM model was also compared with SPWM balanced and unbalanced voltage condition. The results show that SVPWM performed better than SPWM. All the results obtained are within IEEE 519 harmonics standard (i.e. THD less than 5%) with nonlinear load under balanced and unbalanced voltage.

KEYWORDS: Shunt active filter, input voltage, harmonics, space vector pulse width modulation, nonlinear load.

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I. INTRODUCTION

Power quality is a thing of concern in the field of power system engineering due to nonlinear characteristic of power electronics equipment such as electrical drives, compact fluorescent lamp, oven among others which inject harmonics into distribution system (Abijit et al., 2016; Chennia et al., 2014). Poor power factor, voltage flicker, bad voltage regulation, voltage sags and swells are some of the examples of the disturbances of power system engineering and this is a result of degradation of power quality caused by harmonics (Suresh et al., 2011; Akash et al., 2016). Harmonics also reduce the life span of electrical appliances and equipments which leads to significant economic losses in term of revenue (Suleiman et al., 2017).

The conventional harmonic reduction is passive power filter and easy way to reduce the harmonic current. However, the capability of Passive power filter to remove all the harmonic distortion point of coupling (PCC) is limited. Some of the drawbacks are bulkiness and frequency resonance with the inductor in the grid which increases the harmonics (Sindhu et al., 2015; Varaprasad et al., 2014).

In recent times Active Power Filters (APF) was introduced and accepted as one of the most common compensation method. APF are switch mode power electronics inverters for harmonic cancellation at PCC so that harmonics free load current is supply to the consumers at PCC (Akash et al., 2016). The strategies use to obtain the reference signal, current controller, the system topology and DC-link voltage determine the effectiveness of shunt active power filter (SAPF) (Chennia et al., 2014; Akash et al., 2015).

Synchronous reference frame (d-q-o) theory, instantaneous real-reactive power (p-q) theory, modified instantaneous (p-q) theory; flux-based controller; notch filter and Artificial Neural Network (ANN) are some of the different harmonics current signal generation strategies that have been used in the literature. (Zahira et al., 2011). Synchronous Reference Frame (SRF) theory widely used for reference signal generation owing to its directness, accuracy and dynamics compared others many methods (Abijit et al., 2016).

Similarly, hysteresis, triangular wave control, dead beat control, Space vector pulse width modulation among others have been established in the literature for switching signal generation (Naresh et al., 2012). Space Vector Pulse Width Modulation (SVPWM) is known for its complexity and higher with rigorous mathematical calculation for switching signal generation (Phuong 2012). SVPWM is one of the best in pulse signal generation because of advantages of low switching loss, wide range of modulation index and less harmonics distortion. It uses the DC link voltage more effectively than others technique (Phuong 2012).

This work presents the design of Shunt Active Power Filter (SAPF) for harmonic reduction. Synchronous reference frame is used for reference signal generation. Space Vector

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Pulse Width Modulation (SVPWM) is used for switching pulse generation. The paper is organized as follows: section one introduce the concept of SAPF, section two details the mathematical equations of SAPF and SVPWM. Section three details the design procedure and implementation, while section four present the results and discussed of the obtained results and section five details the conclusion of SAPF.

II. SHUNT ACTIVE POWER FILTER (SAPF)

An idea of active power filters is to improve the power factor that is caused by consumption of reactive power and to reduce harmonic current in the power supply. (Nalini et al., 2011). The shunt active power filter works by feeding the exert harmonics current extracted in the opposing direction to the grid at PCC. The achievement of active power filter hinged on the method used to generate reference current and the switching method used to control the inverter legs Chelli et al., 2015). The basic configuration of a shunt active filter is shown in Figure 1.

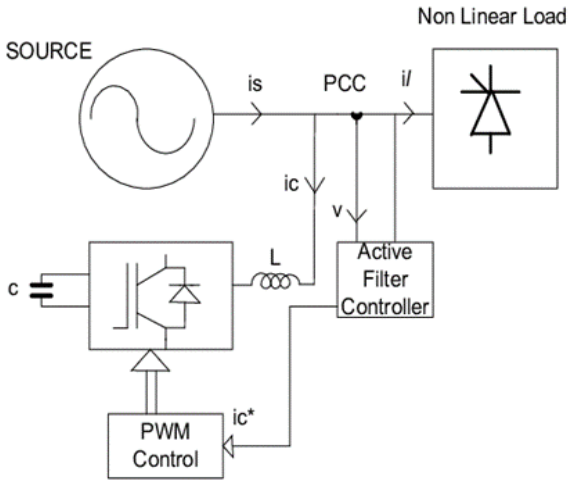


Figure 1: Basic Configuration of a SAPF (Abdeldjabbar et al. 2017)

A. Synchronous Reference Frame (d-q)

The d-q theory transforms three phase voltage and current in a-b-c quantities into d-q in dc quantities (Balasubramaniam et al., 2014). Synchronous reference frame (d-q-0) theory transform from a-b-c to (α-β) using Clark transformation equation and then transform from (α-β) to (d-q-0) using park transformation equation (Hemachandra et al., 2015). The transformation equation is given as follows (Sunitha et al., 2013).

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \cos(\theta-120) & \cos(\theta+120) \\ -\sin\theta & -\sin(\theta-120) & -\sin(\theta+120) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (1)$$

B. Concept of Space Vector Pulse Width Modulation

Space vector pulse width modulation consists of six actives sector and two non-actives sector with reference voltage vector which moves round the states vector. Figure 2 shows the reference vector in the first sector (Phuong, 2012).

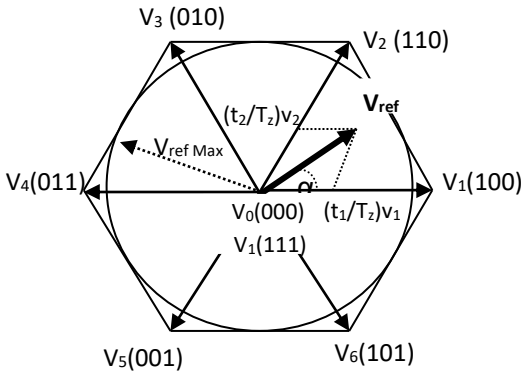


Figure 2: Space Vectors of Three-Phase Bridge Diagram (Thamizhazhagan et al., 2015).

The diagram of a three-phase bridge inverter is shown in the Figure 3. The upper transistors, and determine the current output voltage (Kumar et al., 2012).

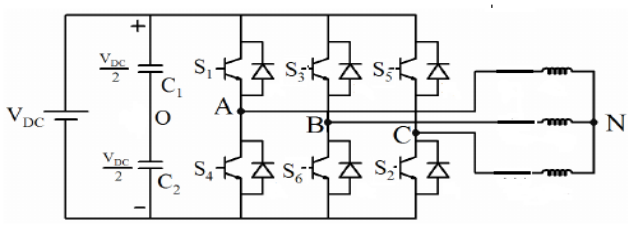


Figure 3: Three Phase Inverter Block Diagram (Phuong, 2012).

Figure 4 shows the eight switching configuration of a three-phase inverter (Kumar et al., 2015).

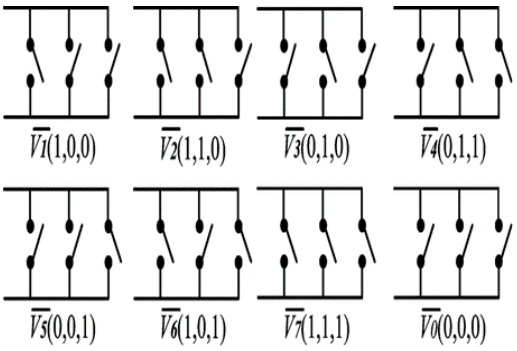


Figure 4: Inverter States (Priyanka et al., 2017).

When the reference voltage vector passes through each sector, different sets of switches in Table 1 will be turned on or off (Phuong, 2012).

Table 1: Space vectors, switching states, and on-state switches (Phuong, 2012).

Space Vector	Switching State	On-state Switch	Vector Definition
$\vec{V}_0$	[000]	S4, S6, S2	$\vec{V}_0 = 0$
$\vec{V}_1$	[100]	S1, S6, S2	$\vec{V}_1 = \frac{2}{3} V_{dc} e^{j0}$
$\vec{V}_2$	[110]	S1, S3, S2	$\vec{V}_2 = \frac{2}{3} V_{dc} e^{j\frac{\pi}{3}}$
$\vec{V}_3$	[010]	S4, S3, S2	$\vec{V}_3 = \frac{2}{3} V_{dc} e^{j\frac{2\pi}{3}}$
$\vec{V}_4$	[011]	S4, S3, S5	$\vec{V}_4 = \frac{2}{3} V_{dc} e^{j\frac{3\pi}{3}}$
$\vec{V}_5$	[001]	S4, S6, S5	$\vec{V}_5 = \frac{2}{3} V_{dc} e^{j\frac{4\pi}{3}}$
$\vec{V}_6$	[101]	S1, S6, S5	$\vec{V}_6 = \frac{2}{3} V_{dc} e^{j\frac{5\pi}{3}}$
$\vec{V}_7$	[111]	S1, S3, S5	$\vec{V}_7 = \frac{2}{3} V_{dc} e^{j\frac{6\pi}{3}}$

The line-to-line voltage vector is given as follows (Irfan et al., 2016).

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (2)$$

Also, the phase voltage vector can be expressed as follows (Irfan et al., 2016).

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (3)$$

III. SYSTEM DESIGN AND MODELLING

A. Selection of DC Voltage

The minimum value of Vdc was calculated using eqn (4).

$$V_{dc} \geq \sqrt{3} V_{pcc-max} \quad (4)$$

Vpcc-max = 400 V

The required minimum of V_{dc} was calculated to be 693 V. Therefore, 700 V was chosen.

B. Selection of Coupling Inductor

The minimum value of interfacing inductor was calculated using eqn (5).

$$Lf \geq \frac{V_{dc}}{12 f sw I_{f\text{-}max}} \quad (5)$$

The converter maximum ripple current = 10 A

V_{dc} = 693 V (for modulation index = 1.7)

Switching frequency = 20 kHz.

The minimum value of L_f was calculated to be 2.88 mH. Therefore, 3 mH was chosen.

C. Selection of DC Capacitor

The minimum value of DC capacitor was calculated using eqn (6).

$$C_{dc} = \frac{2S.n.T}{V_{dc\text{-}max}^2 - V_{dc\text{-}min}^2} = \frac{2S.n.T}{\{(1+z)V_{dc}\}^2 - \{(1-z)V_{dc}\}^2} = \frac{S.n.T}{2zV_{dc}^2} \quad (6)$$

The allowable compensator power transfer is 20 kVA

Number of cycle, n = 0.5 (i.e half cycle)

Period, T for one complete cycle is 0.02 s

Change in V_{dc} of 10% (i.e. z = 0.1)

V_{dc} = 693 V (for modulation index = 1.7)

The minimum capacity of Cdc was calculated to be 2082µF. Therefore, 3000µF was chosen.

D. Shunt Active Power Filter Modeling in d-q

The SRF method is implemented by transforming the three-phase source V_a, V_b and V_c and load current i_a , i_b , and i_c into the three-phase (d-q-0) synchronous reference frame in dc quantities as expressed as follows (Mohammed, 2012).

$$L_f \frac{di_a}{dt} = V_{fa} - R_f i_{fa} - V_{sa} \quad (5)$$

$$L_f \frac{di_b}{dt} = V_{fb} - R_f i_{fb} - V_{sb} \quad (6)$$

$$L_f \frac{di_c}{dt} = V_{fc} - R_f i_{fc} - V_{sc} \quad (7)$$

Eqns (5) to (7) are transformed to synchronous reference frame using equation as expressed as follows:

$$L_f \frac{di_{fd}}{dt} = V_{fd} - V_{sd} - R_f i_{fd} - L_f \omega i_{fq} \quad (8)$$

$$L_f \frac{di_{fq}}{dt} = V_{fq} - V_{sq} - R_f i_{fq} + L_f \omega i_{fd} \quad (9)$$

The currents on the axes d and q are decoupled into two components as follows:

$$U_d = L_f \frac{di_{fd}}{dt} + R_f i_{fd} \quad (10)$$

$$U_q = L_f \frac{di_{fq}}{dt} + R_f i_{fq} \quad (11)$$

Therefore, equation 10 and 11 is re-written as expressed as follows:

$$V_{fd}^* = U_d + V_{sd} + L_f \omega i_{fq} \quad (12)$$

$$V_{fq}^* = U_q + V_{sq} + L_f \omega i_{fd} \quad (13)$$

Eqns (12) and (13) are therefore modeled in Matlab/Simulink.

E. Design of Space Vector Pulse Width Modulation

Space vector pulse width modulation can be implemented by the following steps (Jin-Woo, 2005):

(i) Determination of V_d, V_q, V_{ref} and angle α

(ii) Determination of time duration T_0, T_1 and T_2

(iii) Transistors switching time determination

1.) Determination \of V_d, V_q, V_{ref} and Angle α

Determination of V_d, V_q, V_{ref} and angle α is derived as follows (Jin-Woo, 2005). Consider the sector 1 of the space vector hexagonal diagram in Figure 5.

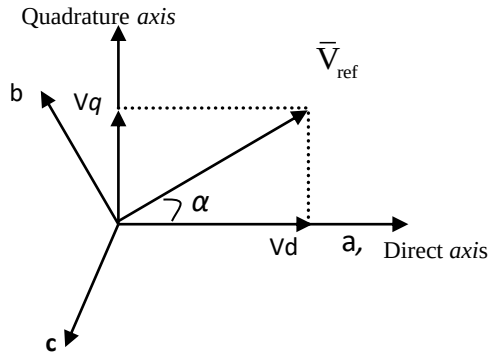


Figure 5: Space Vector in (d- q) Component.

Direct voltage equation and quadrature voltage equation can be written as follows:

$$V_d = V_{a\text{-}n} - V_{b\text{-}n}\cos 60 - V_{c\text{-}n}\cos 60 \quad (14)$$

$$V_q = 0 + V_{b\text{-}n}\cos 30 - V_{c\text{-}n}\cos 30 \quad (15)$$

Eqns (14) and (15) are also expressed as follows:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \quad (16)$$

Also equation of the alpha voltage and beta voltage is given as follows:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \quad (17)$$

Therefore, reference voltage equation and alpha angle are writing as follows:

$$|V_{ref}| = \sqrt{V_\alpha^2 + V_\beta^2} \quad (18)$$

$$\alpha = \tan^{-1}\left(\frac{V_\alpha}{V_\beta}\right) = \omega t \quad (19)$$

where α is the angle between reference voltage and alpha voltage.

Eqns (14), (15), (18) and (19) were written as algorithm in Matlab function in Matlab function block in Matlab/Simulink to calculate V_d, V_q, V_{ref} and angle α.

2.) Determination of time duration T_0, T_1 and T_2

Consider the sector 1 of the space vector hexagonal diagram in Figure 6 (Naresh et al., 2012). The procedures for determining the switching time T_0, T_1 and T_2 is illustrated as follows (Tej et al., 2014; Raul, 2014).

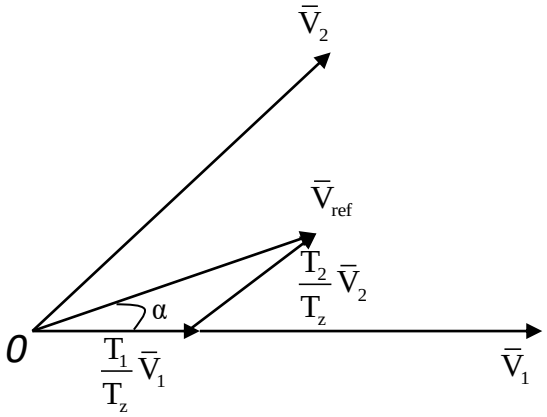


Figure 6: Reference Vector at Sector 1 (Naresh et al., 2012).

The time of switching at any sector is therefore written as follows:

$$T_1 = \frac{\sqrt{3}T_z|\bar{V}_{ref}|}{V_{dc}}\left(\sin\frac{n}{3}\pi\cos\alpha - \cos\frac{n}{3}\pi\sin\alpha\right) \quad (20)$$

$$T_2 = \frac{\sqrt{3}T_z|\bar{V}_{ref}|}{V_{dc}}\left(\sin\left(\alpha - \frac{n-1}{3}\pi\right)\right) \quad (21)$$

$$T_0 = T_z - T_1 - T_2 \quad (22)$$

where,

n = 1 (i.e. sector 1 -6) $\quad 0 \le \alpha \le 60$

Eqns (20), (21) and (22) will be written as algorithm in Matlab function in Matlab/Simulink for sector identification and to calculate T_0, T_1 and T_2.

3.) Transistors switching time determination

The switching pattern of each transistor (S_1–S_6) of the voltage source inverter is therefore configured as shown in Figure 7 (Dev, 2015).

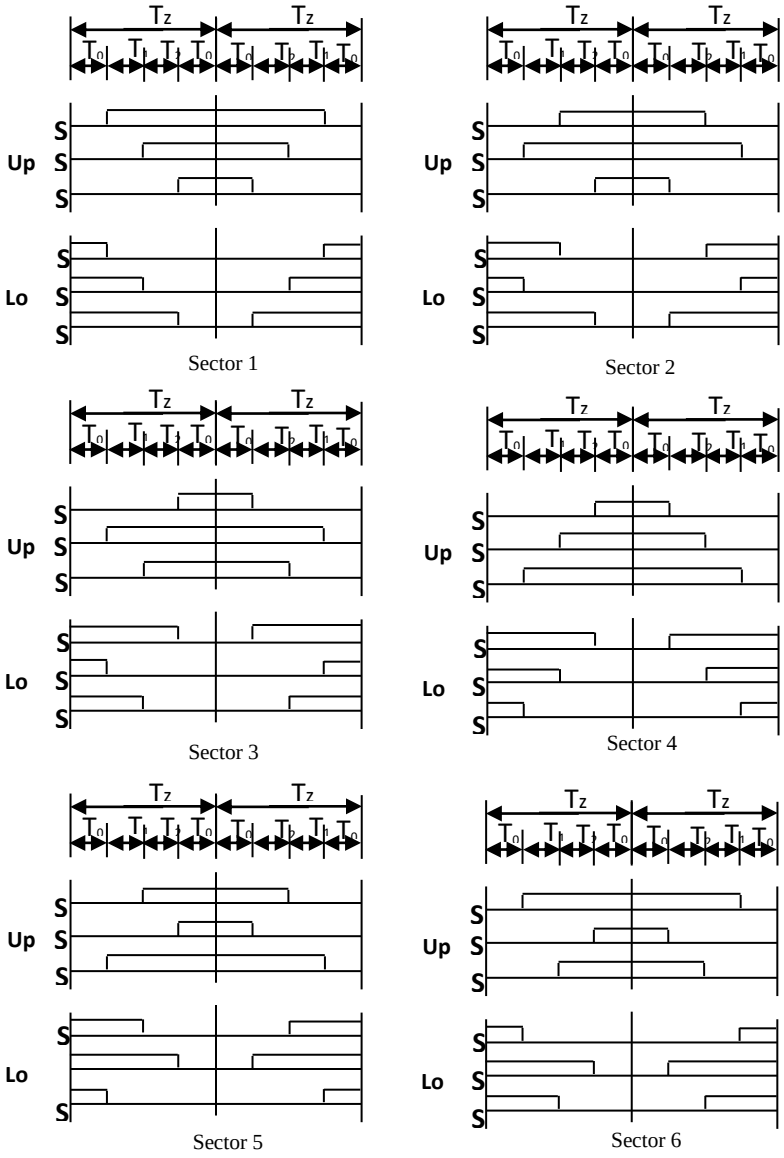


Figure 7: Time of Switching at each Sector Patterns.

III. RESULTS AND DISCUSSION

A. Simulation of RL Load Balanced Loads

Figure 8 shows the waveforms before compensation and after compensation. Figure 8 shows that source current is not an ideal sinusoidal and out of phase with input voltage due to the harmonic current generated by the RL load. The developed SAPF model was tested with RL balanced load condition. Figures 9 shows the simulation waveforms of input Voltage (Vs), Source Current (Is), Compensation Current (Ic) and DC Bus Voltage (V_{dc}). The results show that, the source current (*Is*) is now an ideal sinusoidal and rotates with the same angle with input voltage (*Vs*) when compared with the waveform in Figure 8. The result also shows the waveform of compensation current (*Ic*) injected at the PCC in equal opposing direction to cancel the harmonics present in the load current. The reference DC bus voltage was maintained at 700 V.

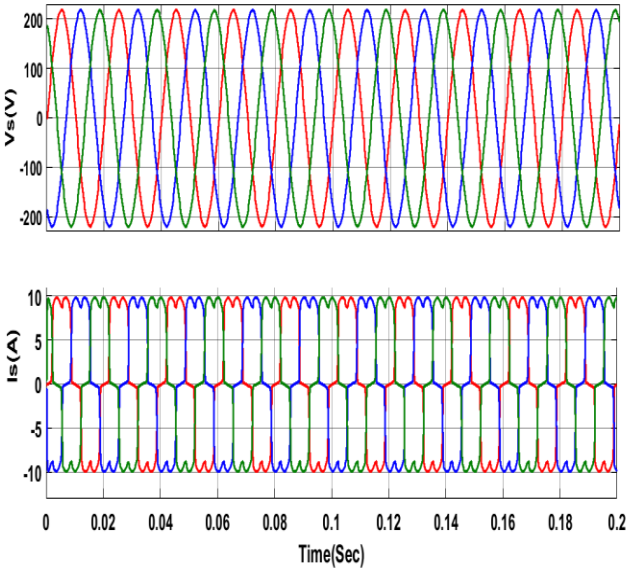


Figure 8: Waveforms of RL Load: Input Voltage (Vs), Source Current before Compensation.

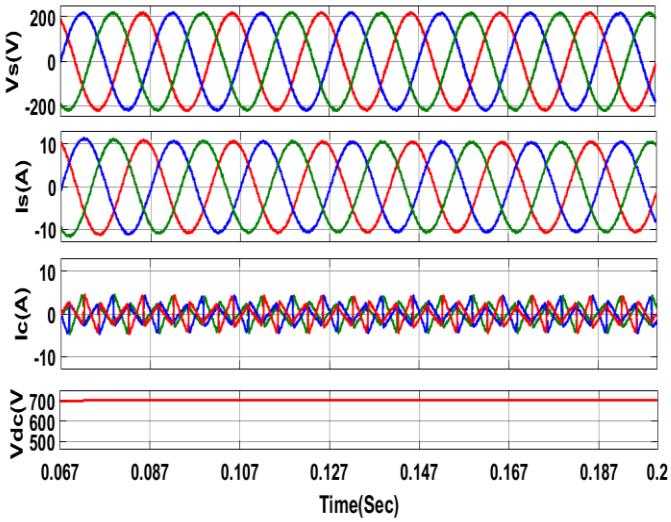


Figure 9: Simulation Waveform of RL Load with SVPWM: Input Voltage (Vs), Source Current (Is) after Compensation, Compensation Current (Ic) and DC Bus Voltage (V_{dc}).

B. Result of FFT Analysis of RL Load (Balanced Voltage)

Figure 10 shows the Fast Fourier Transformation (FFT) analysis of load current before compensation. The THD obtained in Figure 10 is 25.60 % and the fundamental (50Hz) value is 10.4 A. This THD value is large when compared with the IEEE standard harmonic limit (i.e < 5%). The developed SAPF model was subjected to Fast Fourier Transformation (FFT) analysis under balanced voltage with SVPWM. The

result obtained in Figure 11 shows the Fast Fourier Transformation (FFT) analysis of load current after compensation. The result shows a significant 0.91% reduction of THD when compared to 25.6% in Figure 10. Figure 12 shows the Fast Fourier Transformation (FFT) analysis of load current after compensation with SPWM. The result is within the range of IEEE harmonic standard limit of 5%.

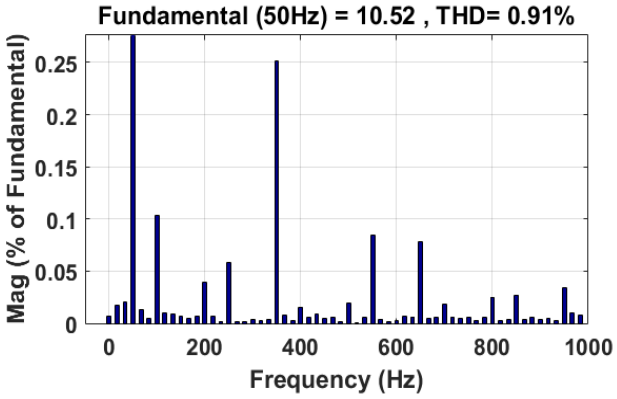


Figure 10: FFT Analysis of Source Current (Is) with RL Load before Compensation.

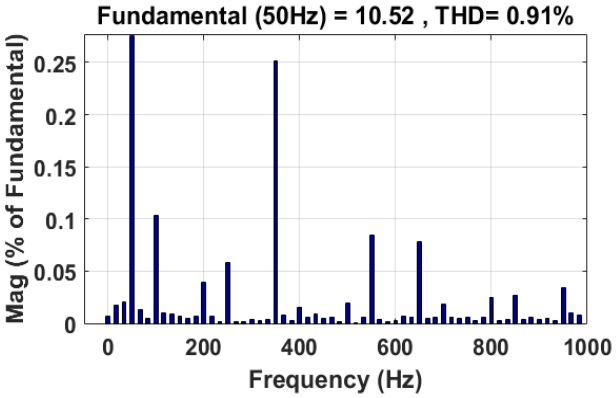


Figure 11: FFT Analysis of Source Current (Is) with RL Load after Compensation.

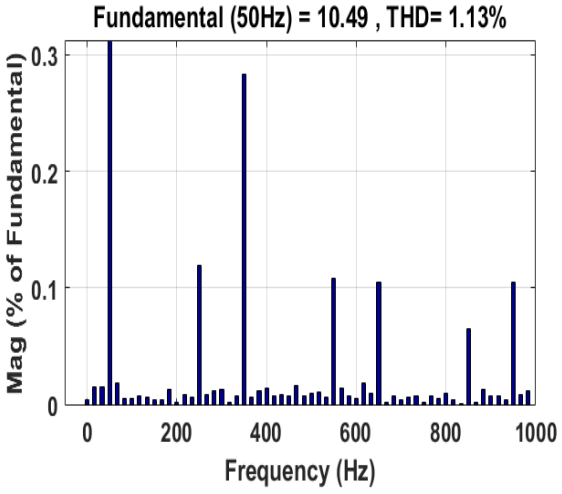


Figure 12: FFT Analysis of Source Current (Is) with RL Load after Compensation.

B. Simulation Result of RL Load

The developed SAPF model was tested with unbalanced input voltage of V_A = 200 V, V_B = 210 V, V_C = 220 V. Figure 13 shows the waveforms before compensation and after compensation. The waveform of the simulation Figure 13 shows that source current is not an ideal sinusoidal due to the harmonic current generated by the combination of RL load and unbalanced voltage. The developed SAPF model was tested with RL balanced load condition. Figures 14 shows simulation waveforms of input Voltage (Vs), Source Current (Is), Compensation Current (Ic) and DC Bus Voltage (V_{dc}). The results show that, the source current (*Is*) is now sinusoidal and rotates with the same angle with the input voltage (*Vs*) when compared with Figure 13. The result also shows the waveform of compensation current (*Ic*) injected at the PCC and the DC bus voltage (*Vdc*). The reference DC bus voltage was maintained constant at 700 V.

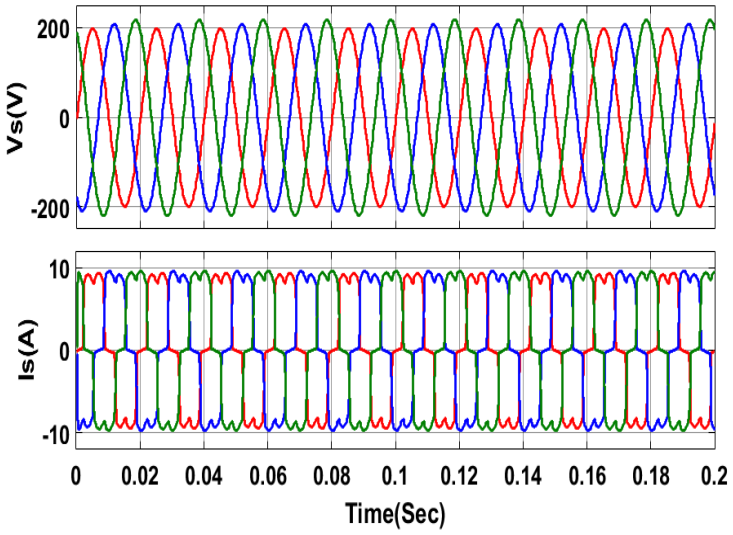
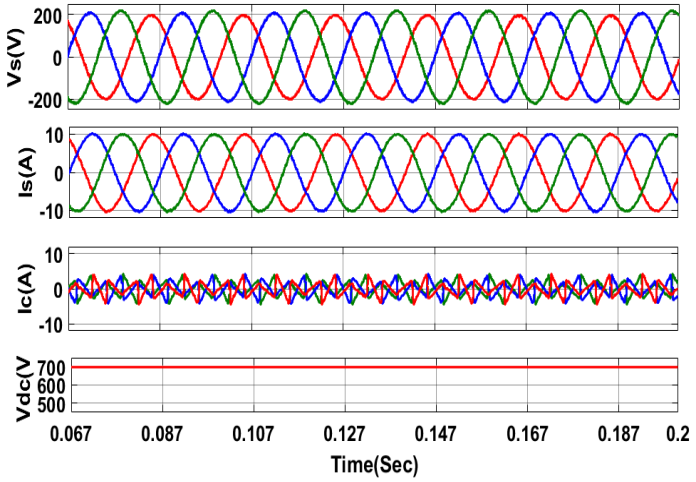


Figure 13: Waveforms of RL Load: Input Voltage (Vs), Source Current before Compensation.



C. Result of FFT Analysis of RL Load

Figure 15 shows the Fast Fourier Transformation (FFT) analysis of load current before and after compensation. The THD obtained in Figure 15 is 26.68 % and the fundamental (50Hz) value is 9.701 A. This THD value is large when compared with the IEEE standard harmonic limit (i.e < 5%). The developed SAPF model was subjected to Fast Fourier Transformation (FFT) analysis under balanced voltage with SVPWM. The result obtained in Figure 16 shows the Fast Fourier Transformation (FFT) analysis of load current after compensation. The result shows a significant 1.74% reduction of THD when compared with 26.80% in Figure 15. Figure 17 shows the Fast Fourier Transformation (FFT) analysis of load current after compensation with SPWM. The result is within the range of IEEE harmonic standard limit of 5%.

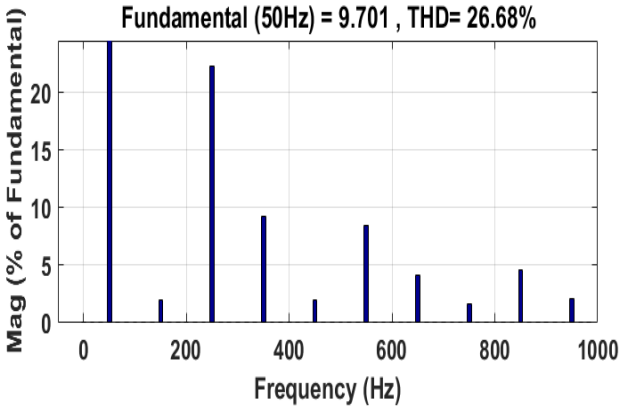


Figure 15: FFT Analysis of Source Current (Is) with RL Load before Compensation.

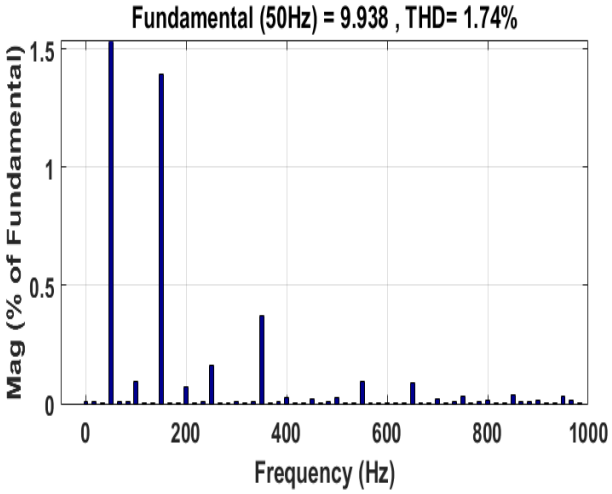


Figure 16: FFT Analysis of the Source Current (Is) after Compensation with SVPWM for RL Load.

IV. CONCLUSION

Shunt Active Power Filter (SAPF) with Space Vector Pulse Width Modulation (SVPWM) based current control method has been developed for harmonic reduction.

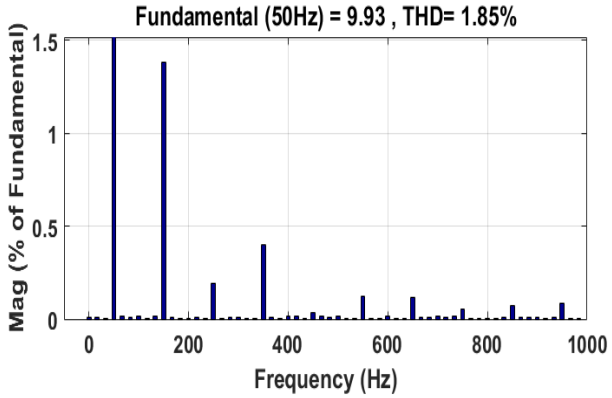


Figure 17: FFT Analysis of Source Current (Is) after Compensation with SPWM for RL Load.

Table 2: Results summary.

Voltage	Control Strategy	THD without SAPF	THDs with SAPF	
			SVPWM	SPWM
Balanced	SRF	25.60	0.91	1.13
Unbalanced	SRF	26.68	1.74	1.85

Synchronous reference frame theory was used to transform ac in a-b-c quantities into DC in d-q quantities and also as control strategy to extract reference harmonic current. The developed model was tested for both RL load under balanced and unbalanced sinusoidal voltage input. FFT analysis shows that harmonic has been reduction from 25.60 % to 0.91 % (THD) for RL nonlinear load for balanced load and 26.68% to 1.74% for unbalanced load using SVPWM. SPWM also reduced harmonic from 25.60% to 1.13% under balanced RL load and 26.68% to 2.47% under unbalanced RL load. The results show that SVPWM performed better than SPWM. The FFT analysis shows that all the results are within the limit of IEEE 519 standard.

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